一种二进制缩放重组电容加权 SAR ADC

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摘　要： 基于 TSMC 180 nm CMOS 工艺，设计了一款 12 位 100 KS/s 低功耗逐次逼近型模数转换器（SAR ADC）.为克服高精度下比较器失调与参考电压抖动对 SAR ADC 性能的影响，采用二进制缩放重组的方法实现电容加权，提高了 SAR ADC 的性能.与传统冗余校准技术相比，在未增加额外的冗余电容的情况下实现了校准的功能，并且保证了输入信号的摆幅.另外，采用低功耗开关切换方式、动态比较器和动态 SAR 逻辑有效降低了功耗.仿真结果表明，在 0.7 V 电源电压下，采样率为 100 KS/s 时，SAR ADC 的有效位数为 11.79 bit，功耗只有 0.95 μW，FOM 值仅 2.68 fJ/conv.

关键词： 二进制缩放重组；电容加权；逐次逼近型模数转换器；低功耗

A binary scaling recombination capacitor weighted SAR ADC

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Abstract： Based on TSMC 180nm CMOS process, a 12-bit 100KS/s low power successive approximation analog-to-digital converter (SAR ADC) was designed. In order to overcome the influence of comparator offset and reference voltage jitter on the performance of high accuracy SAR ADCs, the binary-scaling recombination capacitor weighting method was used to achieve capacitor weighting, which improved the performance of SAR ADCs. Compared to traditional redundant calibration techniques, the calibration was achieved without adding additional redundant capacitors and the swing of the input signal was guaranteed. In addition, using low energy switching method, dynamic comparators and dynamic SAR logic effectively reduced power consumption. The simulation results showed that the ADC achieve a ENOB of 11.79 bit and only consumed 0.95 μW at 100 KS/s sampling rate and 0.7 V supply voltage. And its' FOM value was only 2.68 fJ/conv.

Key words： Binary-scaling recombination; Capacitor weighting; SAR ADC; Low power

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