基于新型 booth 选择器和压缩器的乘法器设计

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摘　要： 为了优化乘法器关键路径延时并减少电路面积，提高乘法器的整体性能.本文在运用基 4booth 算法的基础上，针对部分积生成器延时相对较大的问题，提出了一种新型的 booth 选择器，用于提高部分积生成的效率.同时，本文又提出一种新型的 4-2 部分积压缩器，用于提高部分积压缩器的压缩效率.基于 tsmc28nm 工艺，对运用上述优化点的有符号 16 比特乘法器进行仿真验证和综合，本文设计的乘法器关键路径延时为 0.98 ns.实验结果表明，本文提出的两点新型设计，能较好的提升乘法器的计算性能.
关键词： booth 选择器；4-2 压缩器；乘法器；部分积

Design and implementation multiplier based on new booth selector and compressor

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Abstract： In order to optimize the multiplier critical path delay and reduce the circuit area, improve the overall performance of the multiplier. Based on the Radix 4 booth algorithm, this paper proposes a new type of booth selector for the problem of partial product generator delay, which is used to improve the efficiency of partial product generation. At the same time, this paper proposes a new type of 4-2 partial product compressor to improve the compression efficiency of the partial product compressor. Based on the tsmc 28 nm process, the signed 16-bit multiplier using the above optimization points is simulated and synthesized. The critical path delay of the multiplier designed in this paper is 0.98 ns. The experimental results show that the two new designs proposed in this paper can improve the computational performance of the multiplier.
Key words： booth selector; 4-2 compressor; multiplier; partial product

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