基于 90 nm CMOS 工艺 2.8 GHz 电荷泵锁相环的设计

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摘　要：　为实现超宽带无线收发片上系统中低相位噪声、相互正交的两路本振信号，并避免高集成度环境下发射机中大功率载波信号对锁相环的牵引，本文采用 SMIC 90 nm 工艺设计了一款振荡频率二倍载波频率的电荷泵整数分频锁相环.实现过程中，本文提出了分别在鉴频鉴相器上开关控链路和下开关控制链路上插入传输门的方法，减小死区的同时降低电流失配对环路的影响；采用了低分频系数和高频率的参考信号方案改善了环路的相位噪声；采用了电容阵列的方式来校正压控振荡器方案以减小工艺偏差以及寄生参数对调谐范围的影响.本文完成锁相环版图设计后，提取了各模块的参数并进行了后仿真.SPECTRE 仿真结果表明：该锁相环的相位噪声为-125 dBc/Hz@1MHz，且通过差分二分频可获得两路相互正交的本振信号.

关键词：　锁相环；压控振荡器；鉴频鉴相器

A 2.8 GHz charge-pump phase locked loop in 90 nm CMOS

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Abstract：　In the paper, a charge-pump phase clocked loop with low phase noise in 90nm CMOS, which is used to synthesis two quadrature local oscillator signals, is designed for a UWB transceiver SOC. In the implementation, this paper proposes a method of inserting a transmission gate on the switching link on the phase frequency detector to reduce the dead zone and the influence of the current mismatch. The low division factor and the high frequency reference signal improve the phase noise of the loop. A capacitor array is used to calibrate the voltage controlled oscillator to reduce process variations and the effects of parasitic parameters on the tuning range. After completing the phase-locked loop layout design, the parameters of each module are extracted and post-simulation is performed. The SPECTRE simulation results show that the phase noise of the phase-locked loop is -125dBc/Hz@1MHz, and quadrature signals are produced by the differential 2 divider.

Key words：　phase locked loop; VCO; PFD

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