向下全互连可重构阵列设计与实现

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摘 要：可重构电路的灵活性是电路中的绝对优势，但其电路互连资源有限、PE(Processing Element)资源利用率低.向下全互连可重构阵列结构实现了阵列中每个 PE 与下一行 PE 的全连接，提高了 PE 资源利用率、整体数据处理速度.本设计使用 modelsim、quartus 分别进行了功能仿真、综合下载，结果表明所设计的可重构数据流处理单元能够进行多种配置的可重构.通过验证 FFT 算法在向下全互连的可重构阵列上的映射，结果显示可重构数据流处理单元成功实现了预期功能，并且满足其时序等要求.综合结果显示，4*4 的可重构阵列，包括其外围电路，共占用 19429（58%）门逻辑资源，支持 76.07 MHZ 的工作频率；单个的可重构数据流处理器占用 2565（8%）门逻辑资源，支持最高 108.96 MHZ 的工作频率.

关键词： 向下全互连；动态可重构；FPGA；FFT 算法

Design and implementation of a fully interconnected reconfigurable array

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Abstract：The flexibility of the reconfigurable circuit is an absolute advantage in the circuit， but its circuit interconnection resources are limited， and the utilization of PE (Processing Element) resources is low. The downward fully interconnected reconfigurable array structure realizes full connection between each PE and the next row of PEs in the array， improving PE resource utilization and overall data processing speed. This design uses modelsim and quartus to perform functional simulation and comprehensive downloading. The results show that the reconfigurable data stream processing unit can be reconfigurable in various configurations. By verifying the mapping of the FFT algorithm on the fully interconnected reconfigurable array， the results show that the reconfigurable data stream processing unit successfully implements the expected functionality and meets its timing requirements. The combined results show that 4*4 reconfigurable arrays， including its peripheral circuits， occupy a total of 19，429 (58%) gate logic resources， supporting a working frequency of 76.07 MHz; a single reconfigurable data stream processor occupies 2565 (8%) The gate logic resource supports a working frequency of up to 108.96 MHz.

Key words： full interconnection down; dynamic reconfigurable; FPGA; FFT algorithm

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