

一种复合栅结构 IEGT 器件设计

韩 健, 陈 斌, 顾悦吉

(杭州士兰集昕微电子有限公司, 浙江 杭州 310018)

摘要: 在传统平面栅 IEGT 器件基础上, 设计了一种复合栅结构 IEGT 器件, 器件兼容了电子注入增强和载流子存储层技术. 器件纵向延伸的沟槽栅增加器件有效栅极长度而不额外增加栅极面积, 提高 N-漂移区内部的载流子浓度. 沟槽的存在能够减小 P 型基区侧面的电场强度, 改善由于 N 型阻挡层浓度过高造成的器件耐压的跌落, 从而进一步提高表面载流子浓度, 最终降低器件饱和压降. 器件具有两种不同厚度的栅氧化层, 靠近 P 型基区采用薄栅氧化层以保持器件正常的阈值电压, 其余大部分栅极区域采用厚栅氧化层以降低器件电容, 减小开关损耗.

关键词: IEGT; 沟槽; N 型阻挡层; 饱和压降; 栅氧化层

A new composite gate structure IEGT device design

HAN Jian, CHEN Bin, GU Yue-ji

(Hangzhou Silan Multchip Circuits Co., Ltd, Hangzhou 310018, China)

Abstract: Based on traditional planar gate IEGT device, a new composite gate structure IEGT device was designed. The device is compatible with electron injection enhancement and carriers storage technology. The longitudinally extending trench gate of the device increases the effective gate length without increasing gate area, and carrier concentration inside the N-drift region is increased. The existence of the trench can reduce the electric field of the side of the P-type base, improve the breakdown voltage falling because of high concentration of the N-type barrier layer, and increase surface carrier concentration to reduce device saturation voltage drop. The device has two different thicknesses of the gate oxide, the gate oxide near the p-type base region adopts a thin gate oxide to maintain the device's normal threshold voltage, and the rest of gate region uses thick gate oxide to reduce the device capacitance which is useful to reduce the switching loss.

Key words: IEGT; trench; N-type barrier; saturation voltage drop; gate oxide

作者简介:

韩 健 男, (1983-), 硕士研究生, 工程师. 研究方向为功率半导体器件研发.

E-mail: hanjianhdu@163.com.

陈 斌 男, (1987-), 硕士, 工程师. 研究方向为半导体器件仿真.

顾悦吉 男, (1983-), 硕士, 工程师. 研究方向为功率半导体器件.