基于 SOC 的三模冗余纠错系统设计及实现

陈 锋   1，2 ，张 磊   2 ，宫永生   2

（1 中国科学院大学，北京 100049；2 中国科学院空间应用工程与技术中心，北京 100094）

摘　要：针对航天领域逐渐开始使用的 SOC 器件的 DDR 缓存容易在空间应用环境下发生数据错误的问题，本文设计并实现了一种三模冗余纠错系统，目的是保证空间应用环境下 SOC 器件 DDR 缓存数据的正确性.本系统通过硬件电路的形式进行三模冗余表决，并把表决结果写回 DDR 相应的缓存地址空间.既减少了对 CPU 资源的占用，又提高了表决速度.本设计提出了一种反馈纠错机制，区别于一般的三模冗余能容错但不纠错的特性，能快速地、批量地进行数据纠错.并通过 Xilinx 公司的 XC702 开发板验证，当开发板的 DDR 注入错误数据后，本设计可以成功地在开发板上进行系统容错并纠正源地址的错误数据.达到了确保 SOC 器件 DDR 缓存正确性的目的.

关键词：SOC；TMR；容错；纠错

Design and realization of TMR error correction system based on SOC

CHEN Feng   1，2 ，ZHANG Lei   2 ，GONG Yong-sheng   2

(1 University of Chinese Academy of Sciences，Beijing 100049，China;

2 Technology and Engineering Center for Space Utilization，Chinese Academy of Sciences，Beijing 100094，China)

Abstract：Aiming at the problem that DDR cache of SOC devices used in the aerospace field is easy to generate data errors in the space application environment， this paper designs and implements a three-mode redundancy error correction system to ensure the accuracy of DDR cache data in the space application environment. The system carries on the three-mode redundancy voting through the hardware circuit form， and writes the voting result back DDR corresponding cache address space. It not only reduces the CPU resource， but also increases the voting speed. In this design， a feedback error correction mechanism is proposed， which is different from the general three-mode redundancy， which can tolerate but not correct errors， and can quickly and in batches correct errors. It is verified through XC702 development board of Xilinx company. After the DDR of the development board is injected with error data， this design can successfully carry out the system fault tolerance and correct the error data of the source address on the development board. The accuracy of the SOC device DDR cache is ensured.

Key words：SOC; TMR; errors tolerance; errors correction

作者简介：

陈　锋　男，(1992-)，硕士研究生.研究方向为 FPGA 部分动态重配置.E-mail:chenfeng16@csu.ac.cn.

张　磊　男，(1971-)，硕士，高级工程师.研究方向为卫星通信.

宫永生　男，(1984-)，博士，副研究员.研究方向为空间数据存储.