基于新型压缩器的乘法器设计

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摘　要：为了优化乘法器的延时以及功耗，提高乘法器的性能，针对乘法器的部分积压缩部分设计了新型的压缩器以及新型的压缩算法，在此基础上设计实现了新型的 18 位乘法器.新型压缩器针对常规压缩器横向进位占用延时过大的的特点，通过优化横向进位传递方式来缩短延时；新型的压缩算法采用二叉树结构进行并行处理，与常规的树结构相比，其布线简单，结构规则.基于 simc 40 nm 工艺，对 18 位乘法器进行综合.经过仿真验证，该乘法器关键路径延时 2.43 fs，优于同类乘法器.

关键词：Booth 算法；压缩器；压缩算法

Design of multiplier based on new compressor

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Abstract：In order to optimize the delay and power consumption of the multiplier, a new compressor and a new compression algorithm are designed for the partial product compression part of the multiplier. Based on this, a new design of 18 bit multiplier is proposed and implemented. The new compressor reduces the delay by optimizing the lateral carry path for the characteristic that the conventional compressor has a large time lag for lateral carry. The new compression algorithm uses a binary tree structure for parallel processing, and compared with the conventional tree structure, its wiring is simple and its structure is regular.

Key words：Booth algorithm; compressor; compressed algorithm

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